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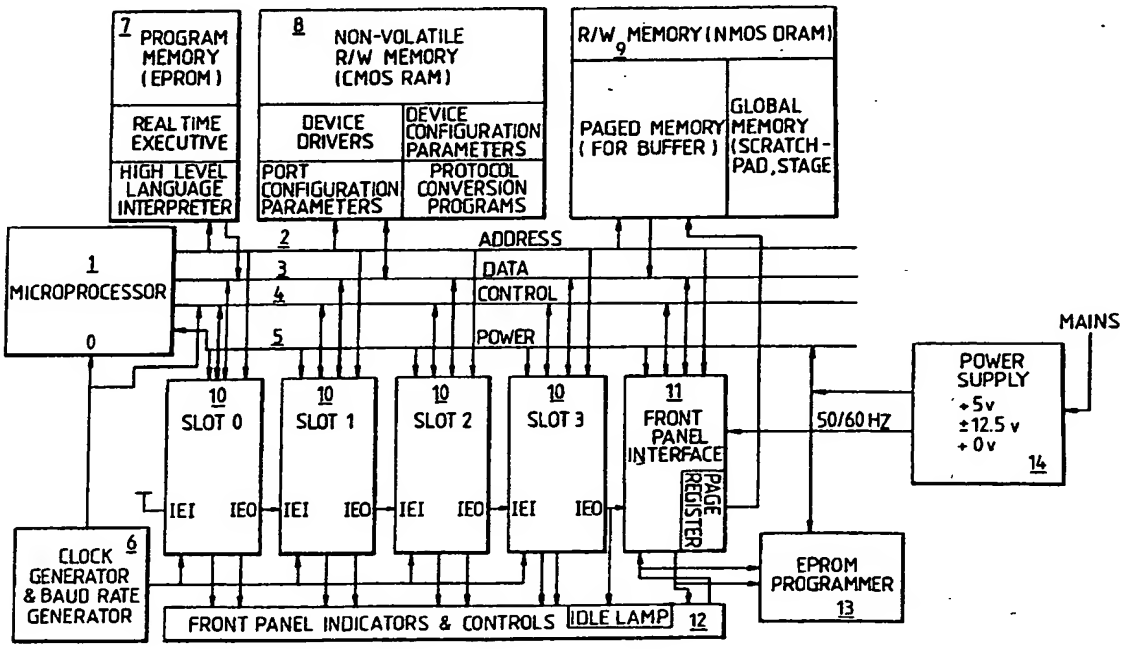

(57) Abstract

A data buffer/switch box comprising a plurality of input/output interface cards (10) removably connected to a motherboard, the data buffer/switch box including circuitry for a plurality of different interface cards provided on the motherboard, and memory means (18) on the motherboard for storing device driver software for each type of interface card (10) connected to the motherboard.

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DATA BUFFER/SWITCH

The present invention relates to a data buffer/switch device for enabling a number of computers or computer terminals to share one or more devices such as computer peripherals or computer ports.

With the increasing use of computers in offices and, more particularly, the increasing use of personal computers, there exists a need to avoid expensive duplication of printers and other equipment such as modems etc. by enabling plural computers to share the same resource. This problem is partly addressed in the case of printers and modems by the provision of data buffer/switch boxes which enable a number of computers having the same type of output port to feed data to one or more printers or modems, switching between the computers being controlled automatically by the buffer/switch box so as to allow immediate use of a printer or a modem by any computer when it is free, but otherwise queuing the printing requests in order.

There are many different interface protocols by means of which computers communicate with, for example, printers, each of which requires a different type of interface and very different signal conditioning. Common interface standards are RS-232C, Parallel Centronics, IEEE-488, IBM 3270, and RS-449. There are other interface standards which are also used, but which are less common. Different computers use different ones of these interface standards for communications with attached devices and therefore, where there are computers of different types wishing to share the same device, some means is required to enable the buffer/switch

box to be able to communicate with the different interfaces of the different computers.

In the past this requirement has been met by a buffer/switch box having a predetermined number of dedicated input/output ports, the interface standards of the individual input/output ports being fixed. Such a device can avoid duplication of circuitry which is common to two or more ports, but suffers from a lack of flexibility in use as it cannot be re-configured to allow for changes in the equipment being used to access the printer. In order to provide a measure of flexibility the number of input/output ports needs to be much greater than is actually required for most applications in order simply to provide sufficient numbers of ports with the different interface standards that may be expected.

A second approach to the problem, favoured usually for more expensive/elaborate systems, is a modular approach in which the buffer/switch box includes a main printed circuit board, known as a motherboard, and a plurality of interface printed circuit boards or cards which connect with the motherboard. Each of the interface cards may provide circuitry for a different interface standard and the motherboard is provided only with the circuitry which is necessary to provide signal conditioning common to all of the interface cards. In practice, the motherboard contains little circuitry as there are few functions common to the widely different interface standards and therefore a particular configuration which is populated with several identical cards will duplicate circuitry on the cards needlessly. Typical duplication will include unusual power supply requirements, a clock generator and device driver program storage.

According to a first aspect of the present

invention a data buffer/switch box comprising a plurality of input/output interface cards removably connected to a motherboard, includes circuitry for a plurality of different interface cards provided on the motherboard, and memory means on the motherboard for storing device driver software for each type of interface card connected to the motherboard.

Thus, not only does the motherboard contain circuitry which is common to all the interfaces, but also circuitry which is common to groups of interfaces, thus reducing duplication whilst at the same time allowing the use of varying numbers of interfaces of different types, thus maintaining the benefits of a modular approach.

The data buffer/switch box may be utilized as a printer sharing device, enabling plural computers to use on or more printers, but may be used in a wide range of other applications, for example enabling computer port sharing by plural terminals and any other circumstance in which a data switch would be useful, including modem sharing, LAN node sharing, etc, etc. In particular, there are considerable advantages to be obtained by using the same box simultaneously as a VDU multiplexer and a printer switch.

In particular, it is envisaged that at least the Centronics Parallel and RS-232C Serial interface requirements will be provided on the motherboard as these are the most common interfaces used, but the requirements of other interfaces will also be provided as required.

Conventionally, data buffer/switches of the modular type with plural interface cards or computers with multiple interface cards incorporate the device driver software on the interface cards themselves as the software is specific to each type of interface card. However, this means that with several

identical cards there are several identical copies of the driver software. Furthermore, a substantial part of the usual address bus is needed on each interface card to permit the memory to be addressed, and more memory address space is used up than is necessary as each interface has to be assigned sufficient space for the largest anticipated driver device. Alternatively, a complex memory paging scheme must be used. A further problem is that integrated circuit components having memories of the required small size, typically 256 to 1024 bytes are no longer being made.

The present invention proposes further that only one copy of each device driver program that is required is provided on an EPROM. This is then loaded into non-volatile RAM on the motherboard when the respective interface card requiring this driver software is added or incorporated into the buffer/switch box and the EPROM is then removed. Thus, one non-volatile RAM chip can hold all the device drivers, in addition to various configuration parameters etc that may be required. Each device driver program then uses up only as much memory and memory address space as it really needs.

Data buffer/switch boxes enable a computer to send data to be transferred to the buffer/switch box which then stores or "buffers" the data and sends it to the device as required, the storing of the data in the buffer/switch box releasing the computer from the transfer operation and thus enabling a further task to be carried out on the computer. In those cases where the interface is truly bi-directional buffering occurs in both directions. Conventionally, buffer/switch boxes assign a predetermined amount of buffer memory to each input port. This is disadvantageous as, at any one time, only a small proportion of the total buffer memory may be used if

only a small number of computers are sending data to the buffer. Recently, systems have appeared which offer dynamic, that is to say variable, allocation of buffer memory, achieving this by assigning pages of memory, each of typically 256 bytes, to each input port, the number of 256 byte pages being able to be increased as buffer memory is added to the buffer/switch box.

According to a second aspect of the present invention, buffer memory is divided into a fixed number of pages, regardless of the amount of memory in the buffer, the size of each page being arranged to be increased as the buffer memory size is increased. This is achieved by suitable software control and has several advantages in terms of the speed at which the software can execute.

In order to provide for use of RS-232C Serial interfaces the motherboard needs to incorporate a clock generator whereby the baud rate for any particular interface card may be chosen from one of a number of standard frequencies. Each interface may require one or (less commonly) two of these frequencies. Conventionally, a baud-rate clock generator has been provided for each input/output channel, but this is expensive and envitably causes duplication of circuitry. A second approach to the problem is to supply all the possible required frequencies to each interface card from the mother board and to provide for selection of the particular required frequency on each interface card. Whichever of these methods is chosen selection is by means of switches which themselves add significantly to the cost.

According to a third aspect of the present invention, the motherboard incorporates a baud rate clock generator that outputs all the commonly required frequencies and provides these on a row of

pins; each RS232-C interface card having an at least four-way connector comprising two pairs of pins, a first pair for determining the baud rate of transmission from the interface card and a second pair for determining the rate of transmission to the interface card, a wire link being provided to connect pins of the first and second pairs together if the transmit and receive baud rates are to be the same; and a connecting lead connectable to the requisite pin on the clock generator and to one of the pins of the at least four-way connector.

By this means, if the relevant frequency desired for an interface is already in use from the clock generator (so that the pin is not available for attachment to the lead from the interface card, the lead may be attached to a spare pin on the interface card having the relevant frequency supplied to it. The arrangement provides that there will always be such a spare pin to which the lead from a second interface card may be connected and so on.

If different transmit and receive frequencies are required on an interface card then the wired jumper link may be removed and a second lead used in the same manner as the first. In this way a split baud rate may be offered to the interface card input/output port.

Preferably, each of the interface cards has a first and a second input/output port and the at least four-way connector is a six-way connector, the third pair of pins of which determine the transmit/receive rate of the second port, and wire jumpers being provided as required for connection to pins of the first and second pairs of the connector.

The advantage of this system is that a single baud rate generator with multiple outputs is much less expensive than multiple generators with single outputs, wire leads are simple, cheap and more

versatile than switches and a split baud rate can be provided to intput/output ports very simply.

A further problem with the RS-232C interface standard is that although it is meant to be a standard, the way that the standard is interpreted varies considerably from one piece of equipment to another.

One example of a device constructed in accordance with the present invention will now be described with reference to the accompanying drawings in which:-

Figure 1 is a block diagram of the motherboard;

Figure 2 is a circuit diagram of the relevant part of an RS-232C interface card; and,

Figure 3A and 3B are circuit diagrams of a parallel Centronics interface card showing the input mode and output mode usage respectively.

With reference first to Figure 1, the motherboard has a microprocessor 1 with an address bus 2, a data bus 3 and a control bus 4, supplied with power via a power bus 5, and a master clock signal from a clock generator 6.

Attached to the buses are read-only program memory 7 (EPROM), some non-volatile (CMOS RAM) memory 8, some read/write memory 9 (NMOS DRAM), several slots 10 for interface cards adhering to various protocols, and a front-panel interface 11.

The read-only memory 7 consists of one or more EPROMs, containing a real-time executive and optionally a high-level language interpreter. The real-time executive provides standardised software interfaces to the device drivers required for each of the interface cards, and implements the logic associated with allocation and de-allocation of the paged buffer memory.

The non-volatile memory 8 is implemented in low-power CMOS RAM, and is provided with a battery

(not shown) to ensure that there is no data loss during power-down. It contains one device driver for each type of interface, port and device configuration parameters associated with each port and device, and optionally protocol conversion programs written in the high-level language for interpretation by the interpreter.

Inclusion of the device driver software in the non-volatile memory has the advantages already documented.

The read-write memory 9 is implemented in NMOS DRAM and is structured in the way described as the second aspect of the invention above.

In particular it should be noted that there are two conflicting requirements that arise when a microprocessor is required to address a greater amount of memory than is available in its normal address space. Thus, a paging system is necessary to access the bulk of the memory, whereby a page register is set to select some of the address lines, and the microprocessor address bus is used for the remainder.

However, this means that there is no memory that is always available, regardless of the contents of the page register. For microprocessors that have no internal read/write memory, this poses problems, as virtually all microprocessors require some scratchpad area, and a stack. The stack, in particular, must occupy a contiguous area of memory, and must be accessible without regard to the page register contents. In the device of this example an address scheme is implemented in which the 20 address lines from a 1 megabyte block of memory are mapped into two address spaces. The microprocessor sees two 4096-byte blocks, at E000-EFFFh and F000-FFFFh. The latter is mapped so that it appears as a contiguous block of memory.

Thus, a portion of it is always available to the microprocessor for use as a scratchpad and stack, and a portion of it is selected by means of a page register, which is actually implemented as part of the front-panel circuitry.

The address line mapping of global memory at F000-FFFFh is:

Processor		Memory
A0	.....	A0
|	.....	|
A7	.....	A7
A8	.....	A9
|	.....	|
A11	.....	A12
A12	.....	=1
|	.....	|
A15	.....	=1

Using this scheme, the contiguous address space is present at F000-FFFFh, regardless of whether the unit is populated with 64, 256, 512, 768 or 1024K bytes of memory (A8 is absent for 64K DRAMs).

Conversely, when the microprocessor refers to page E000-EFFFh, microprocessor address line A12 will be zero, and that selects the following mapping (where Rn is a bit from the page select register):

Processor		Memory
A0	.....	A0
|	.....	|
A7	.....	A7
A8	.....	A8
A9	.....	A17
A10	.....	A18
A11	.....	A19
R0	.....	A9

R7	A16
A12	=0
A13	=1
A14	=1
A15	=1

The result of this is that regardless of the amount of memory present, there will always be 256 pages selected by R0..R7. However, the size of these pages will be proportional to the amount of memory available, ie 256 bytes/page for 64K, 4096 bytes/page for 1Mb.

The memory locations used for the contiguous memory at F000-FFFFh will also appear in the paged memory, as the first 256 bytes of each of the first 16 pages.

The front panel interface 11 drives the front panel indicators, polls the front panel buttons 12, and generates a periodic interrupt once every mains cycle, to implement a realtime clock. As no front panel interface is required during EPROM programming 13 and reading, the front panel interface controls this function as well so that device driver software can be loaded from EPROM into non-volatile memory.

Two additional front panel indicators are driven directly by signals offered by each interface port (regardless of the type of the interface).

The interface slots 9 provide a standard hardware interface, to which cards may be attached to provide support for many possible communication protocols.

All necessary control signals from the microprocessor are provided on the slot connector, along with an interrupt chain implemented via IEI/IEO. Only a very small number of address lines needs to be provided, since no software needs to

reside on the interface card.

In order to minimise the cost of this flexibility, certain features that are the most likely to be required are implemented on the motherboard.

By providing a standardised hardware and software interface which is nevertheless sufficiently flexible to cope with any protocol that may be required, the optimum tradeoff is achieved between cost and flexibility.

In particular, the clock frequencies required for supporting RS-232C are provided for any interface that needs them, by the master clock generator 6. Additional power supplies are also made available by the power supply circuit 1. Additional functions which the power supply implements include a signal at mains frequency for implementation of the real-time clock, a power on reset signal and a lockout signal for the non-volatile memory (to prevent data corruption during power-up/down), and special voltage levels needed during EPROM programming.

Turning now to Figure 2, the interface card circuit illustrated provides an unusual solution to the problem of non-standard pinout of RS-232C.

The left-hand hand side of the diagram is quite conventional, and provides a means for a Dual Universal Asynchronous Receiver/Transmitter chip (DART), U3, to be supported by a microprocessor. The right-hand half of the circuit is duplicated for each channel. The functions of the two halves are identical, and only one will be described. The component designations on the diagram in brackets refer to the secondary channel. (Only the primary channel component designations will be used in this description).

A switch SW3 permits the user to choose a pin configuration which broadly complies with the

requirements for either DCE or DTE. This circuit has the unusual advantage that SW3 only requires four poles, despite controlling eight pins on the interface.

The top two poles of this switch simply effect the swapping over of the serial data pins, 2 and 3.

In addition to the above-mentioned serial data pins, the interface must also support at least one flow control line in each direction. (This is used to indicate to the remote device one's readiness to accept data.) In this example, one line is provided in each direction, namely, the pin labelled DTR on U3 (to output this device's readiness to accept data) and the pin labelled CTS (to test the remote device for readiness for data).

In this circuit, the flow-control output is only offered to one pin. In the DCE case, this is always pin 5. D4 and R19 provide isolation from pins 6 and 8.

In the DTE case, usage is divided roughly 3:2 in favour of pin 20 over pin 4. However, both must be offered, and a jumper J1 is provided to permit this selection. In this case, D3 and R17 perform the isolation function from pins 11,19.

The flow-control input is more difficult. There is very poor agreement about the pin to use in either the DCE or DTE case. However, one can be sure about the relevant voltage levels, namely, that a voltage more negative than -3v indicates Not-Ready-For-Data, whereas a voltage more positive than +3v indicates Ready-For-Data.

The method adopted of connecting a resistor and diode in series with each pin which may be used in this way, means that the common point will be pulled to a negative voltage if any of the connected pins is at a negative voltage. Any pins at a positive voltage, and those that are not connected, do not

affect the result. Thus any of these pins will function for indicating readiness for data. The only compromise associated with this scheme is that a device that offers one of these pins permanently negative will be unable to receive data until that pin is disconnected.

It is a requirement of RS-232C/V.24 that inputs that are not connected should not have a voltage present on them. To this end, R15/16 are provided, to ensure that this is the case.

The DCE/DTE selection of flow-control input is effected by D1, D2 and SW3d. The relevant group of input pins is connected to the input U5 pin 4 by the diode. The inactive group is connected to +12v. This performs a dual function of ensuring that the other diode (D2/1) is turned off, so that those pins cannot participate in the flow control, and also puts a positive voltage on the various pins that might otherwise be assumed to be flow-control outputs, namely pins 11,19 for the DTE case, and pins 6,8 for the DCE case.

A six pin connector CN3 is provided to enable plural baud rate frequencies to be supplied from the baud rate generator 6 on the motherboard to the transmit line TA of the primary channel, the receive line RA of the primary channel and the transmit/receive line TRB of the secondary channel, by means of flying leads L1, L2. Jumpers J3 are also provided.

It will be appreciated that if TA,RA and TRB all require the same frequency than a single flying lead L1 from the appropriate pin of the baud rate generator 6 on the motherboard is all that is necessary, the jumpers J3 being connected to supply the same frequency to the TA and TRB lines. If a further interface card requires the same frequency then its flying lead can be connected to the spare

pin on this card, and so on.

If the TA,RA and TRB lines require different frequencies then plural flying leads can be connected back to the baud rate generator. Again the spare pin on each line will allow a further interface card to receive the same baud rate without requiring multiple pins on the baud rate generator.

Figures 3A and 3B illustrate the circuit of a bi-directional fully-buffered Centronics Interface card for attachment to the motherboard. This card is unusual, as it uses the same circuitry in different ways for input and output. The two figures illustrate the two modes of use, in each case all detail irrelevant to the operation in this mode has been omitted.

The pulse generator comprises U6b, U4a, U7d and C1, R4. Its mode of operation is to generate a negative-going pulse, of duration defined by R4, C1, whenever a positive edge occurs at the output of U6b.

During output, the pulse generator is used to generate the STRobe- pulse, indicating that the data is avilable on the data bus. R12 and C7 ensure that the data has time to become stable on the bus, before the STR- is sent.

On output, it is necessary to acknowledge receipt of the data from the PIO, and this is done via R6,C2 and U6a.

When functioning as an output, the BUSY line is simply monitored prior to sending data, via R7, C3, U6d, U4c.

When functioning as an input, the BUSY becomes an output line, indicating readiness to receive the next byte. In this mode, BUSY is asserted on the falling edge of the incoming STR-, via D1,C6,U7b,U5b,U8c. On the rising edge of STR-, the data is clocked into the PIO, and as a result, the PIO denies ARDY. This propagates after a short while

to BUSY via U6b. However, in the meantime, BUSY has been kept high due to the time constant of R3,C6. BUSY will then remain asserted until the microprocessor has time to read the data byte received.

On output, PRIME- functions directly as a control output, via U8a. (The connection via U5a, U7a, U6a is an unwanted side-effect, but which has no impact on operation.)

On input, it is necessary to register that PRIME- has gone low, even if it only occurred for a very short time. Therefore, a latch has been implemented. The operation of this is as follows:-

Initially, PRIME- is high, and as a consequence, U6c output is high, and PIO0 A3 input is low.

If PRIME- is pulled low by the remote equipment for at least timeconstant R8, C5, U6c output will go low, and as a result, U4b will permit PIO0 A3 to float high (pulled by R13). This causes open-collector gate U8a to turn on, pulling PRIME- permanently low (even after the initial stimulus has been removed).

As the falling edge of PRIME- is seen, U7a finds both inputs high for time R5C4, and generates a pulse rather like STR- pulse, and causing an interrupt to the processor, via PIO1, as for receipt of a normal character. This causes the processor to read the status, and establish that a PRIME- pulse has occurred.

The processor then attempts to reset the PRIME- capture latch as follows:

It re-defines PIO0 A3 as an output. It pulls it low, and then restores it to being an input. Assuming that the stimulus from the remote device has now gone (i.e. it is no longer pulling PRIME- low), this will have the effect of resetting the latch.

The processor again interrogates the status of A3, and if it finds that it is low, the reset has been successful. If it finds that it is still high, it assumes that the stimulus is still active, and sets a timeout, after which it comes back to try again.

CLAIMS

1. A data buffer/switch box comprising a plurality of input/output interface cards (20) removably connected to a motherboard (30), the data buffer/switch box including circuitry for a plurality of different interface cards provided on the motherboard, and memory means (8) on the motherboard for storing device driver software for each type of interface card connected to the motherboard.

2. A data buffer/switch box according to claim 1, wherein the motherboard contains circuitry which is common to all the interface cards and also circuitry which is common to groups of interface cards, thus reducing duplication whilst at the same time allowing the use of varying numbers of interfaces of different types.

3. A data buffer/switch box according to claim 1 or claim 2, wherein device driver software for the Centronics Parallel and RS-232C Serial interface protocols is provided on the motherboard.

4. A data buffer/switch box according to any one of the preceding claims, wherein only one copy of each device driver software is provided on the motherboard.

5. A data buffer/switch box having a buffer memory (9) divided into a fixed number of pages, regardless of the amount of memory in the buffer, the size of each page being arranged to be increased as the buffer memory size is increased.

6. A data buffer/switch box according to claim 5, wherein the size of each page of buffer memory is controlled by resident software.

7. A data buffer/switch box comprising a plurality of RS-323C serial input/output interface cards removably connected to a motherboard, wherein the motherboard incorporates a baud rate clock generator that outputs all the commonly required frequencies and provides these on a row of pins; each RS232-C interface card having an at least four-way connector comprising two pairs of pins, a first pair for determining the baud rate of transmission from the interface card and a second pair for determining the rate of transmission to the interface card, a wire link being provided to connect pins of the first and second pairs together if the transmit and receive baud rates are to be the same; and a connecting lead connectable to the requisite pin on the clock generator and to one of the pins of the at least four-way connector.

8. A data buffer/switch box according to claim 7, wherein each of the interface cards has a first and a second input/output port and the at least four-way connector is a six-way connector, the third pair of pins of which determine the transmit/receive rate of the second port, and wire jumpers being provided for connection to pins of the first and second pairs of the connector.

Fig. 1.

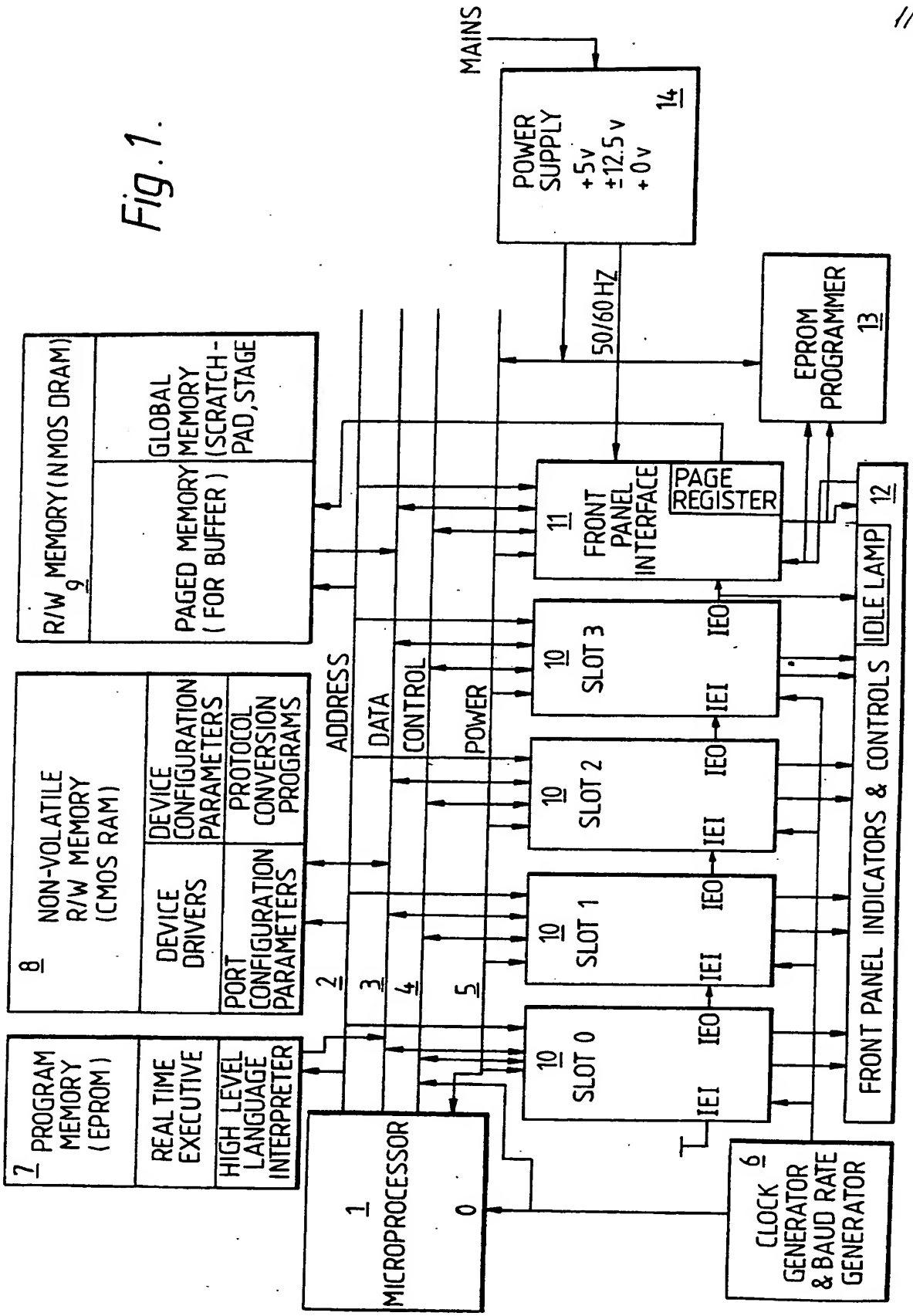
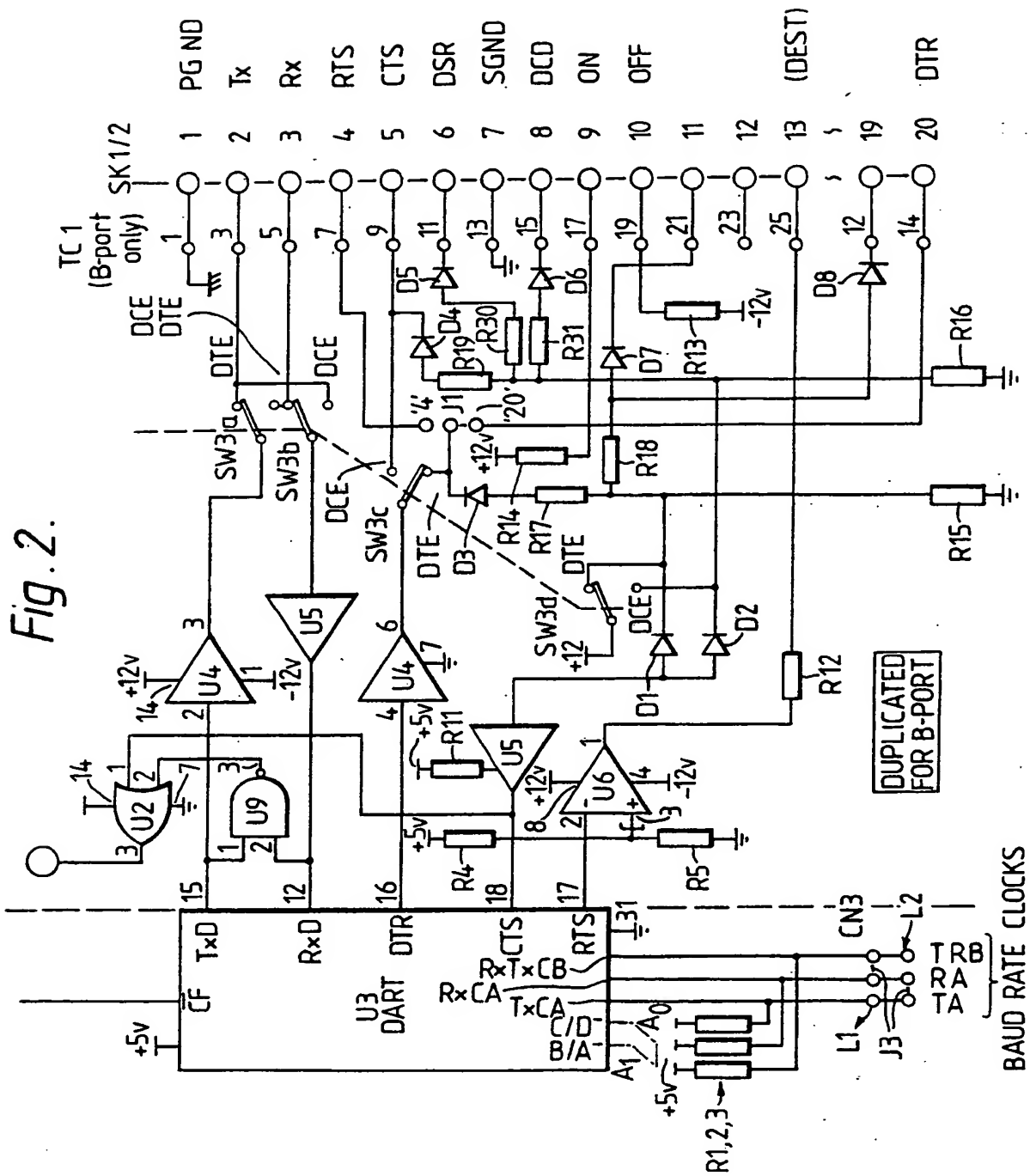

MAINS
POWER SUPPLY
+5v
±12.5v
+0v
14
50/60HZ
EPROM PROGRAMMER
13
R/W 9 MEMORY (NMOS DRAM)
GLOBAL MEMORY (SCRATCH-PAD, STAGE
PAGED MEMORY (FOR BUFFER)
11 FRONT PANEL INTERFACE
PAGE REGISTER
12
IDLE LAMP
8 NON-VOLATILE R/W MEMORY (CMOS RAM)
DEVICE CONFIGURATION PARAMETERS
PROTOCOL CONVERSION PROGRAMS
DEVICE DRIVERS
PORT CONFIGURATION PARAMETERS
ADDRESS
DATA
CONTROL
POWER
2
3
4
5
10 SLOT 3
10 SLOT 2
10 SLOT 1
10 SLOT 0
IEO
IEI
7 PROGRAM MEMORY (EPROM)
REAL TIME EXECUTIVE
HIGH LEVEL LANGUAGE INTERPRETER
1 MICROPROCESSOR
0
6 CLOCK GENERATOR & BAUD RATE GENERATOR
FRONT PANEL INDICATORS & CONTROLS

Fig. 2.


PG ND
Tx
Rx
RTS
CTS
DSR
SGND
DCD
ON
OFF
(DEST)
DTR
SK1/2
TC 1
(B-port only)
DCE
DTE
SW3a
SW3b
SW3c
SW3d
U2
U3
DART
U4
U5
U6
U9
D1
D2
D3
D4
D5
D6
D7
D8
R4
R5
R11
R12
R13
R14
R15
R16
R17
R18
R19
R30
R31
J1
CN3
L1
L2
J3
TRB
RA
TA
BAUD RATE CLOCKS
DUPLICATED FOR B-PORT
TxD
RxD
DTR
CTS
RTS
RxCB
TxCB
RxCA
TxCA
C/D
B/A
A1
A0
CF
+5v
+12v
-12v
R1,2,3

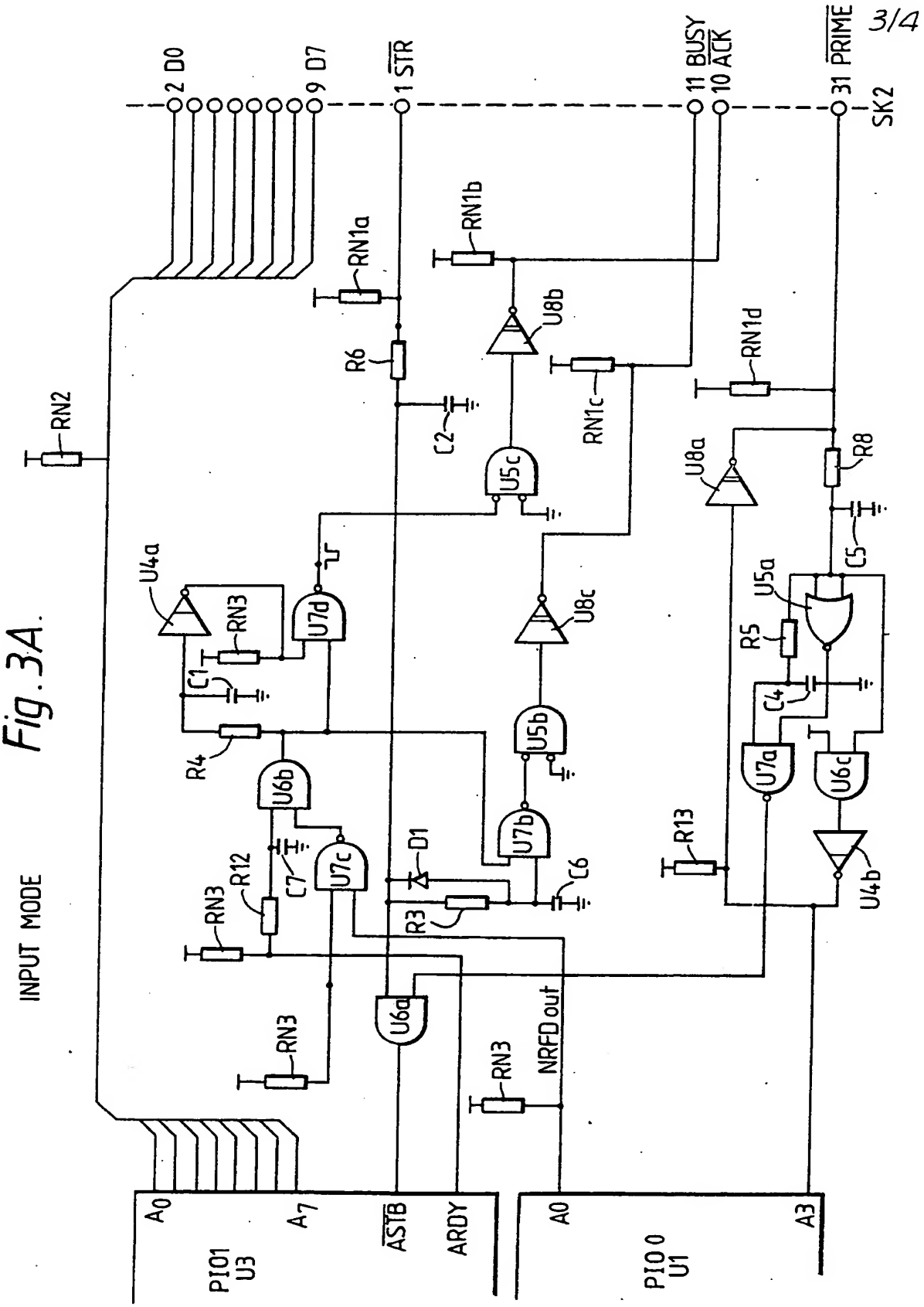


Fig. 3A.

INPUT MODE

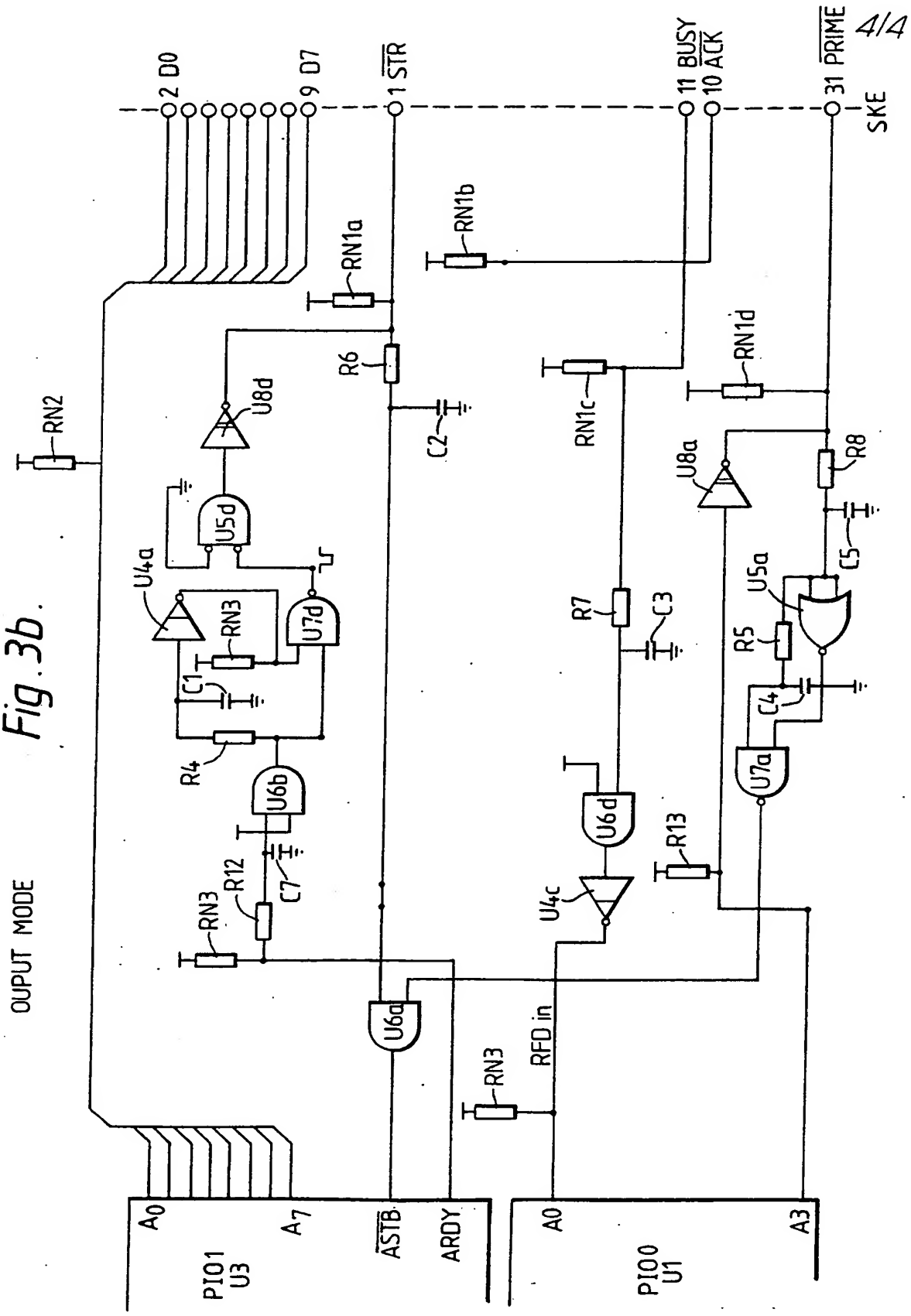

2 D0
9 D7
1 STR
11 BUSY
10 ACK
31 PRIME
SKE
RN1a
RN1b
RN1c
RN1d
RN2
R6
C2
U8d
U5d
U4a
RN3
U7d
C1
R4
U6b
R12
C7
U6a
U6d
U4c
R13
U8a
R8
C5
U5a
R7
C3
R5
C4
U7a
OUPUT MODE
RFD in
A0
A7
ASTB
ARDY
PIO1
U3
A0
A3
PIO0
U1

Fig. 3b.

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(74) Agent: GILL JENNINGS & EVERY; 53/64 Chancery Lane, London WC2A 1HN (GB).

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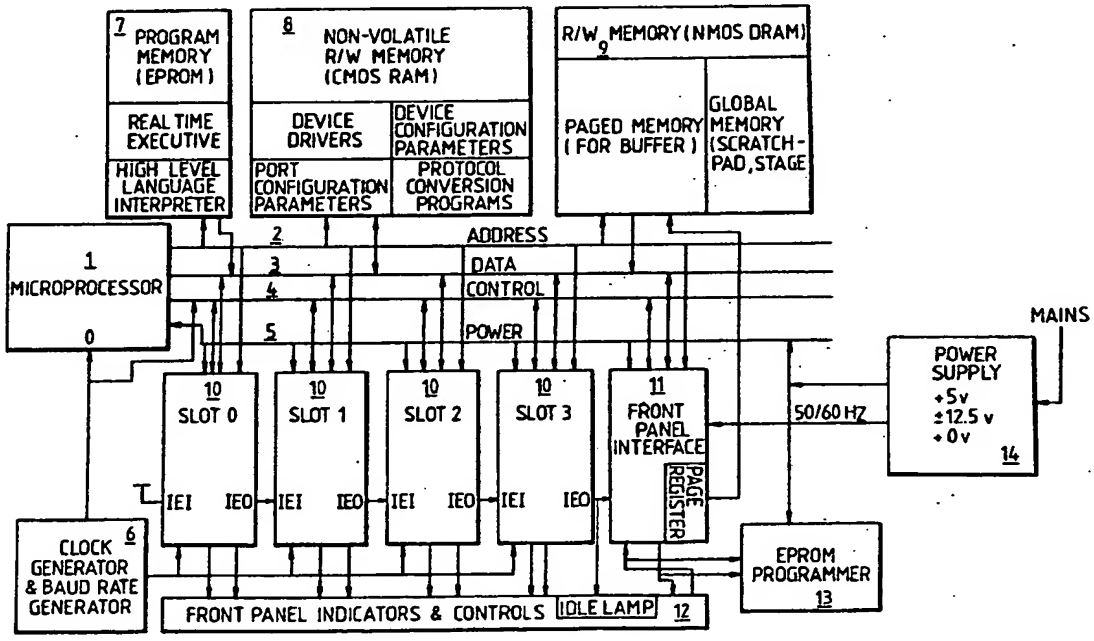
(54) Title: DATA BUFFER/SWITCH



(57) Abstract

A data buffer/switch box comprising a plurality of input/output interface cards (10) removably connected to a motherboard, the data buffer/switch box including circuitry for a plurality of different interface cards provided on the motherboard, and memory means (18) on the motherboard for storing device driver software for each type of interface card (10) connected to the motherboard.

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INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 87/00792

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 13/38; G 06 F 5/06; G 06 F 12/06

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 06 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 4293909 (R.D. CATILLER et al.) 6 october 1981 see column 2, lines 25-39; column 2, line 66 - column 3, lines 1-16, and lines 23-30; column 4, lines 42-51, 59-66; column 5, lines 58-68; column 6, lines 1-8; column 7, lines 33-49; column 10, lines 16-25;; column 20, lines 16-25; figures 1,4A	1,2
Y		7,8
A		3,4
	--	
X	IBM Technical Disclosure Bulletin, volume 21, no. 7, December 1978, (New York, US), D.M. Nagel et al.: "Programmable communications subsystem having controller incorporating micro-processor", pages 2633-2645 see figures 1-5; page 2633, last line; page 2635, paragraph 2; page 2636, lines 1-20; page 2639, last paragraph	1,2

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* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
25th May 1988	29 JUN 1988
International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	P.C.G. VAN DER PUTTEN

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
Y		7,8
A		3,4
	--	
Y	US, A, 4079452 (K.N. LARSON et al.) 14 March 1978 see figures 3,4,6; column 1, lines 18-55; column 2, lines 17-39, 46-53; column 3, lines 62-66; column 4, lines 50-64; column 5, lines 57-64; column 6, lines 19-30, 41-49; column 8, lines 18-22	1,2,7,8
	--	
X	Patent Abstracts of Japan, volume 6, no. 75 (P-114)(953), 12 May 1982, & JP, A, 5713561 (HITACHI SEISAKUSHO K.K.) 23 January 1982 see abstract and figures	5
	--	
A	The 4th Annual Symposium on Computer Architecture, 23-25 March 1977, Long Beach, IEEE, (New York, US), A.C. Parker et al.: "Hardware/ software tradeoffs in a variable word width, variable queue length buffer memory", pages 159-164 see page 159, paragraph II; page 161, paragraph "Program mode"; page 162, figures 4a and 4 b	5,6

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers....., because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim numbers....., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim numbers....., because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☒ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

- claims 1-4,7-8 : Universal protocol adaptor with motherboard realisation
- claims 5-6 : Variable page size control

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☒ No protest accompanied the payment of additional search fees.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. GB 8700792 SA 19319

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 13/06/88
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4293909	06-10-81	None	
US-A- 4079452	14-03-78	FR-A- 2355332	13-01-78
		DE-A- 2726811	29-12-77
		JP-A- 53016542	15-02-78
		GB-A- 1573046	13-08-80
		GB-A- 1573047	13-08-80
		CA-A- 1105585	21-07-81